In the Claims:

Claim 1 (currently amended): A semiconductor device including a field-effect transistor, said field-effect transistor comprising:

a semiconductor layer including a source region, a drain region and a channel region between said source region and said drain region;

a gate insulating layer formed on said channel region; and

a gate electrode structure formed on said gate insulating layer including~~;~~,

a Si nano crystal layer formed on said insulating layer,

a poly-SiGe layer formed on said Si nano crystal layer~~;~~,

a thin interfacial oxide layer formed on said poly-SiGe layer sufficiently thin to cause minimum resistance to current flow and with sufficient [O] to block Ge~~;~~, and

a layer of poly-Si formed on said thin interfacial layer.

Claim 2 (original): The semiconductor device as set forth in Claim 1 wherein said Si nano crystal layer comprises crystal grain sizes of less than 100nm in diameter.

Claim 3 (original): The semiconductor device as set forth in Claim 2 wherein said poly-SiGe layer has a [Ge] of up to at least 70%.

Claim 4 (original): The semiconductor device as set forth in Claim 1 wherein a layer of $CoSi_2$ is formed on said layer of poly-Si.

Claim 5 (currently amended): The semiconductor device as set forth in Claim 1 wherein said thin interfacial oxide layer has a thickness of 3 to 4~~A~~ Å.

Claim 6 (original): The semiconductor device as set forth in Claim 1 wherein said gate electrode structure acts as a gate electrode for both n-channel field effect transistors and p-channel field effect transistors.

Claim 7 (currently amended): A field effect transistor having an SiO_2 gate insulating layer and a multi-layered gate electrode structure formed on thereon, comprising:

a Si nano crystal seed layer formed on said SiO_2 insulating layer with the grain size of said Si nano crystals of said Si nano crystal layer being less than 100~~A~~ Å;

a layer of poly-SiGe continuously formed upon said Si nano crystal seed layer;

a thin discontinuous interfacial oxide layer formed on said layer of poly-SiGe that allows current flow and has sufficient [O] to block upward Ge diffusion;

a layer of poly-Si formed on said interfacial layer; and

a metal silicide layer formed on said layer of poly-Si.

Claim 8 (original): The field effect transistor as set forth in Claim 7 wherein said thin discontinuous interfacial layer is SiO_2 or $Si_xGe_yO_z$.

Claim 9 (original): The field effect transistor as set forth in Claim 7 wherein said thin discontinuous interfacial oxide layer is 2 to 4~~A~~ Å thick.

Claim 10 (original): The field effect transistor as set forth in Claim 9 wherein the [Ge] in said layer of poly-SiGe is up to 70%.

Claim 11 (canceled)

Claim 12 (original): A method for fabricating the gate electrode of a field effect transistor device, comprising the steps of:

providing a semiconductor layer having at least one gate insulating layer region on a portion of said semiconductor layer;

forming a Si nano crystal layer on said gate insulating layer;

forming a poly-SiGe alloy layer on said Si nano crystal layer;

forming an oxide layer on said poly-SiGe layer sufficiently thin so as to offer little resistance to current flow and sufficient [O_y] to block upward Ge diffusion upon heating; and

forming a poly-Si layer on said oxide layer.

Claim 13 (original): The method as set forth in Claim 12 wherein said Si nano crystal layer is formed 3 to 6 nm thick with a grain size of 20 to 150A in diameter.

Claim 14 (original): The method as set forth in Claim 13 wherein said Si nano crystal layer is formed ex situ by spin-on of Si nano crystal from solution.

Claim 15 (original): The method as set forth in Claim 12 wherein the [Ge] in said poly-SiGe alloy layer is up to at least 70%.

Claim 16 (original): The method as set forth in Claim 12 wherein said Si nano crystal layer and said poly-SiGe alloy layer are formed in situ by rapid thermal chemical vapor deposition.

Claim 17 (original): The method as set forth in Claim 12 wherein said oxide layer is 3 to 4A thick.

Claim 18 (original): The method as set forth in Claim 17 wherein said oxide layer is formed by an in situ purge of the rapid thermal chemical vapor deposition chamber in an oxygen ambient at 300 to 500°C.

Claim 19 (original): The method as set forth in Claim 12 including the steps of conformally depositing a layer of Co upon said poly-Si layer and said doped regions adjacent thereto and applying heat to said semiconductor layer to activate said doped regions and form $CoSi_2$ on said poly-Si layer and said doped regions.

Claim 20 (original): The method as set forth in Claim 19 wherein said semiconductor layer having at least one gate insulating layer region comprises at least two gate insulating layer regions with one gate insulating layer region formed on a p-type well and the other formed on an n-type well and wherein said p-type well is ion implanted with phosphorous or arsenic and said n-type well is ion implanted with boron so that said step of applying heat activates said phosphorous or arsenic and said boron with said Ge in said poly-SiGe enhancing said activation of boron.

Claim 21 (new): A field effect transistor including a SiO_2 gate insulating layer and a multi-layered gate electrode structure formed thereon, said gate electrode structure comprising:

a Si nano crystal seed layer formed on said SiO_2 insulating layer with the grain size of said Si nano crystals of said Si nano crystal layer being less than 100Å;

a continuous poly-SiGe layer formed upon said Si nano crystal seed layer;

a poly-Si layer formed on said poly-SiGe layer,

a thin discontinuous interfacial oxide layer formed on said layer of poly-Si that allows current flow and has sufficient [O] to block upward Ge diffusion;

a layer of poly-Si formed on said interfacial layer; and

a metal silicide layer formed on said layer of poly-Si.